ABSTRACT

A multi-lane link that automatically detects if the lanes in the link have been reordered and corrects the order of the lanes. In one embodiment, the link includes a transmitter and a receiver. The receiver is configured to receive a plurality of lanes and includes a receiver logic circuit configured to receive signals from each of the plurality of lanes. Lane misordering is corrected during a training sequence in which a first training sequence and a second training sequence are bilaterally transmitted between the transmitter and receiver. The receiver monitors the training sequence for symbols that are unique to each lane and if an unexpected symbol is detected in the lane, the receiver logic circuit will correct the order of the lanes. The link further comprises a transmitter logic circuit configured to transmit signals to the lanes. The transmitter logic circuit is configured to reorder the sequence of the signals transmitted to the lanes if the transmitter does not detect a response from the receiver. The transmitter logic circuit may consist of a bank of multiplexers configured to transmit a selected one of two input signals to be transmitted through a lane. Similarly, the receiver logic circuit may comprises a bank of multiplexers configured to transmit a selected one of two input signals received from a lane. The unique lane identifiers symbols are preferably insensitive to binary inversion and are preferably 10-bit symbols compatible with an 8B/10B encoding scheme.